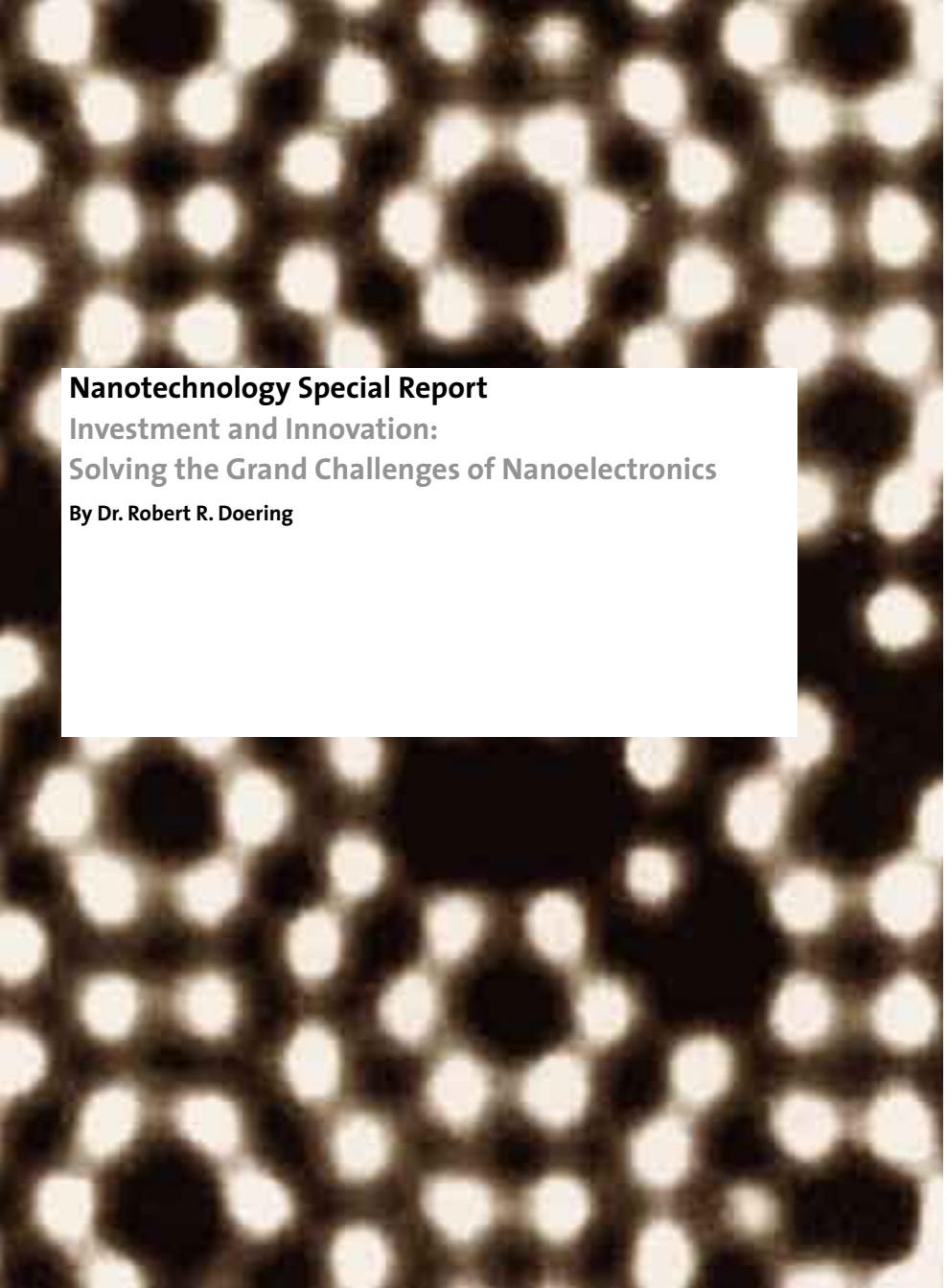


Nanotechnology Special Report

Investment and Innovation: Solving the Grand Challenges of Nanoelectronics

By Dr. Robert R. Doering

Many of the hottest topics in scientific research today fall under the broad umbrella of nanotechnology. Such research strives to create useful new materials and devices so small that their features are measured in nanometers—billionths of a meter.

It only takes three or four atoms side-by-side to span a nanometer. Thus, nanotechnology is sometimes characterized as "working at the atomic or molecular scale." Using traditional chemistry techniques, we have been able to synthesize molecules from atoms for a long time—and this is still part of nanotechnology.

What's new, in part, is a larger bag of tricks for placing atoms where we want them. We are also interested today not just in arranging atoms into molecules (in solution, for example), but also in using them to build macroscopic structures with features of nanometer accuracy. Electronic systems already incorporate this new type of nanotechnology in the form of state-of-the-art semiconductor integrated circuits (ICs).

PACKING MORE PERFORMANCE INTO EVER-SMALLER DEVICES

The very first ICs of 45 years ago contained semiconductor devices with minimum lateral feature sizes on the millimeter scale. Subsequent miniaturization, or scaling, of these devices to ever-smaller dimensions has enabled incredible progress in the performance, energy efficiency, and cost-per-function of ICs. These advances have revolutionized electronics, information technology, and communications.

Since 1992, the SIA has sponsored a consensus-building activity aimed at identifying technical barriers to a continuation of this progress. In 1998, this endeavor became a worldwide collaborative effort known as the International Technology Roadmap for Semiconductors (ITRS).

According to the 2003 roadmap, ICs have already transitioned from the era of microelectronics to nanoelectronics, though many of the manufacturing techniques are still evolving from that previous era. For example, in the 2004 year-of-production "hp90nm technology node" optical lithography and plasma etching have been extended to the point where transistor gate lengths are as small as 37nm and circuit layout is performed on a 1nm grid. The transistor gate is insulated from the underlying silicon substrate by a gate dielectric (currently silicon-oxynitride) barely more than one nanometer thick.

IMAGINING THE INFINITESIMAL

To get a better perspective on these tiny dimensions—and the complexity of the circuits we can build with such nanocomponents—imagine that a 2 x 2cm^2 integrated circuit were linearly enlarged by a factor of one million, so that a nanometer becomes a millimeter (1/25 inch). The magnified chip would then be comparable in size to New York City (the length of Manhattan Island, but about six times wider). On this scale, the transistor gate length becomes 1.5 inches and the circuit layout ("city map") is specified to the nearest millimeter!

There is a lot of room in an area the size of New York City for structures with a width of 1.5 inches. For example, if the chip were entirely static-random-access-memory (SRAM), it would contain more than 2 billion transistors. Dynamic RAM (DRAM) is even denser in terms of bits/cm^2.

Many of the transistors in a chip are organized four-at-a-time into logic gates (not transistor gates) performing basic digital operations such as NOT-AND (NAND).

Today, these gates have switching speeds of less than 10 picoseconds and can be manufactured for less than about 50 microcents each, when integrated into semiconductor chips. The energy required to switch one of them is only about one femtojoule (10^{-15} watt-seconds).

This incredible semiconductor technology that we have today is called CMOS, and it continues to advance at a rapid pace. Since improved IC density, speed, energy efficiency, and cost-per-function have mostly resulted from scaling device dimensions, the overall rate of advancement is often characterized by the time required to halve the circuit area required for a basic logic or memory function—currently about two years.

The entire semiconductor industry conducts vast R&D efforts aimed at extending CMOS technology trends through scaling and other means. However, SIA members agree that continuing this progress for more than another decade or so will require revolutionary breakthroughs.

UNDERSTANDING THE SEMICONDUCTOR INDUSTRY'S GRAND CHALLENGES

A 2003 study by the SIA Technology Strategy Committee (TSC) identified two high-level, technical grand challenges. With significant new federal R&D support, solving both could provide benefits across almost every aspect of our society, including the economy, health care, and national security.

Grand Challenge 1: Create a new nanomanufacturing paradigm

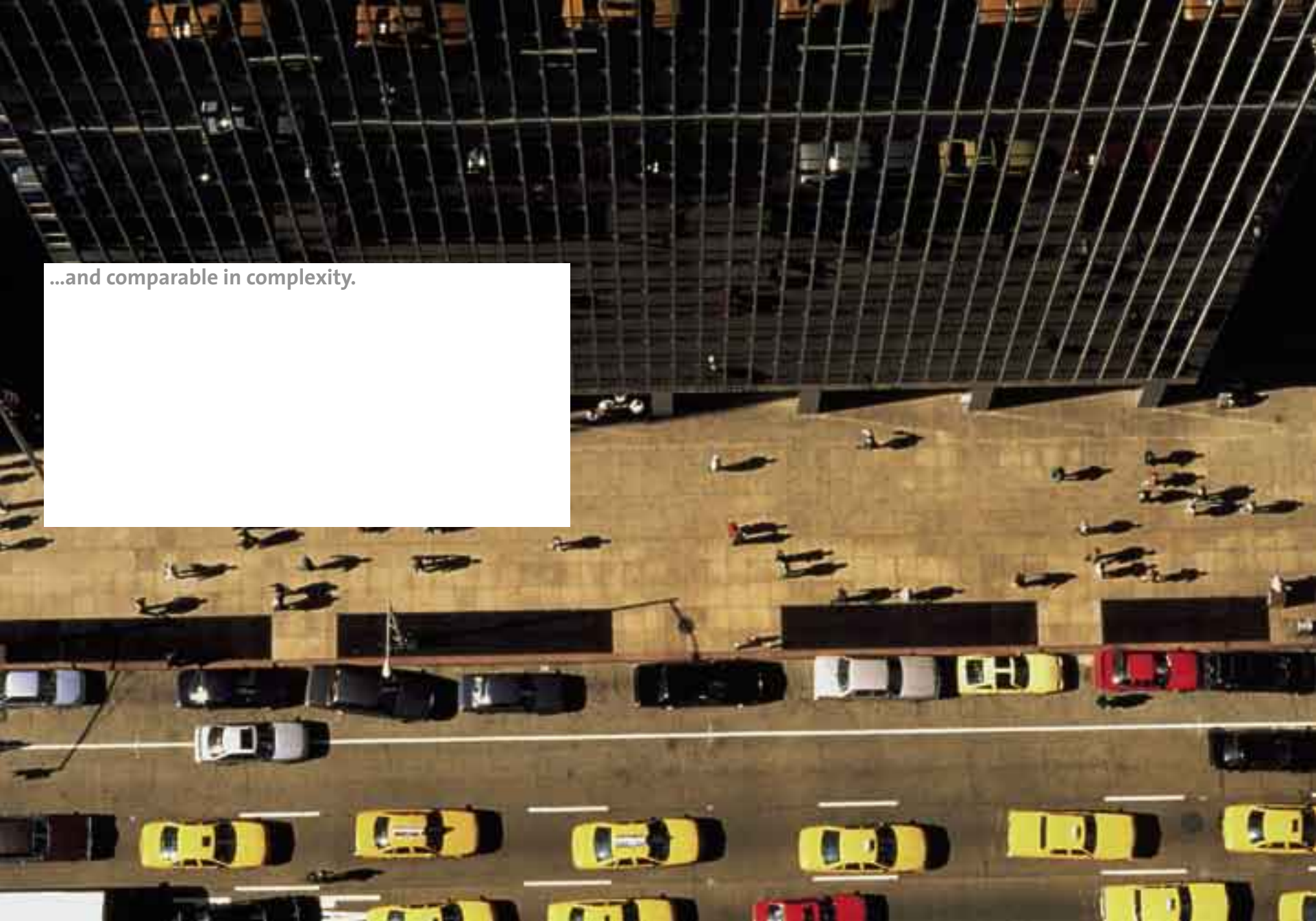
The first of the grand challenges is to develop a new nanomanufacturing paradigm that continues the reduction in cost-per-function (of logic gates or bits of memory, for example) far into the future. Despite significant incremental advances, the traditional masked-lithography of thin-films is becoming so complex that it may not support the favorable cost trend all the way to the device-limit of CMOS scaling, especially for low-volume ICs.

In particular, a future manufacturing approach that lowers the cost of capital equipment, pattern generation, and atomic-level process control is extremely desirable.

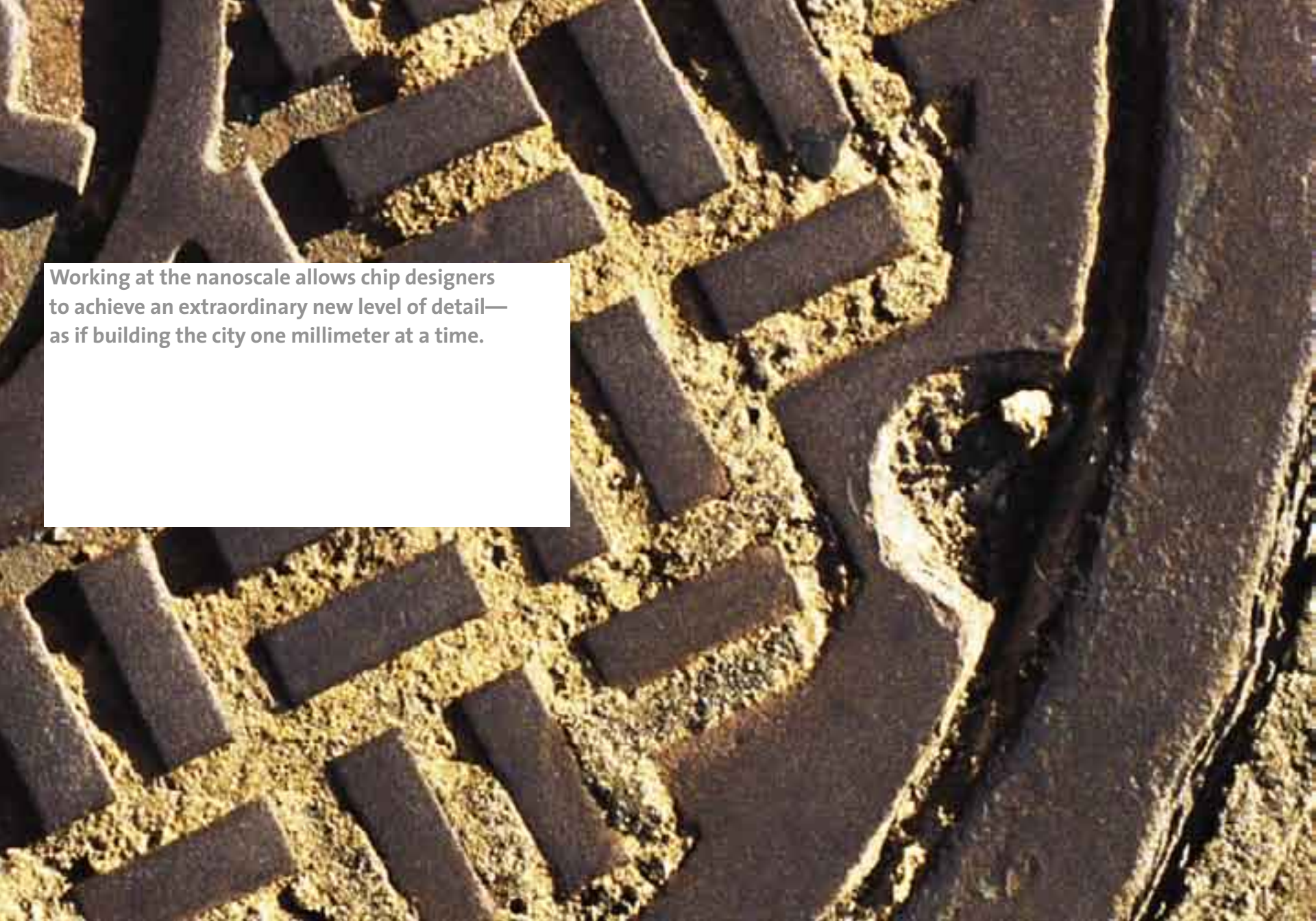
Some solutions to this challenge might be found in the broad area of research on directed self-assembly—possibly even adapting one or more biological techniques. For example, a promising start has been made on bioengineering viruses to fabricate nanoelectronic structures (*IEEE Spectrum*, Nov. 2003, pp. 36-41). Ideally, a suite of such advanced nanomanufacturing methods would be developed that could build a wide variety of devices, including CMOS scaled to its ultimate limits.

Significantly, it is likely that broad-application, commercially viable ultimate CMOS will be limited mainly by volume-manufacturing feasibility and costs rather than by intrinsic device-physics limits. Therefore, a new approach to manufacturing that continued to lower the cost-per-function of CMOS even without further scaling would also be very beneficial.

A nanometer multiplied by one million is a millimeter. If you multiply a large integrated circuit (20mm x 20mm) by one million, it would be roughly the size of New York City...



...and comparable in complexity.



Working at the nanoscale allows chip designers to achieve an extraordinary new level of detail—as if building the city one millimeter at a time.

Nanomanufacturing, however, is unlikely to be a universal construction process. At some level of detail, any new manufacturing techniques will be interdependent on the nature of the devices being fabricated. Thus, process and device researchers will need a continuing exchange of ideas and closer coordination as we move into development engineering on their advanced concepts.

Grand Challenge 2: Develop new devices and circuits

The second grand challenge for nanoelectronics is to develop new devices and corresponding circuits. In this domain, we hope to extend the industry's historical rates of improvement in gate-level metrics—such as energy-delay product and standby power—for at least several more decades.

CMOS is already being scaled to the point that the tradeoff between performance and power consumption forces significant compromise. Thus, recent technology nodes have offered a range of devices optimized from very high speed through very low power.

Uncertainty exists even over the best nomenclature for talking about post-CMOS devices. As CMOS technology is pushed to its limits, it appears it will morph in various ways—with new materials, new geometries, and so on. Some define CMOS as "use of any form of complementary field-effect transistors (FETs)." However, others believe that "CMOS-like terminal characteristics" is a better definition—even if the devices are much more exotic than FETs—since CMOS circuit designs and methodology could essentially be maintained.

THE ANSWERS LIE IN ADVANCED RESEARCH

Terminology aside, significant additional research is required if we are to continue the electronic performance trends of the past few decades. Here's a look at some potential sources for breakthroughs:

- *Medium term*—Over the next 10 to 20 years, these grand challenges might be addressed by device technologies that have already been studied in industrial labs. One example is carbon-nanotube FETs. They are typical of advanced device research in that much more progress is currently being made in exploring their potential electrical characteristics than in overcoming practical issues for implementation into complex ICs, largely a manufacturing problem.
- *Long term*—To further extend information- and signal-processing performance trends for more than the next couple of decades, we need additional research on integrated-circuit components that overcome most of the interconnect charge-transport issues (parasitic capacitance, for example), as well as near-equilibrium thermodynamic constraints that will limit bulk-charge-based technology. Solutions might be found in devices based on state variables other than electric charge. We should especially explore the use of quantum systems such as electron or nuclear spins and molecular or photonic states.

  Initially, such new devices might not be able to replace the full functionality of FETs. In that case, it is likely that they would be hybridized with CMOS into ICs that take advantage of the complementary device characteristics. For example, the new state variable might first be exploited for dense memory in an IC that still employs CMOS logic. Other complementary functions might include sensing, optical I/O, or eventually, quantum computation. In future nanochips, we will probably define nanoelectronics by functionality rather than by the actual state variables employed.

UNLOCKING THE FUTURE REQUIRES COLLABORATION AND FUNDING

Addressing these grand challenges will require substantial long-range, high-risk research, which cannot be conducted exclusively by the semiconductor industry.

Breakthroughs that will bring forth revolutionary nanoelectronics technologies demand new and significantly extended R&D collaborations among government, universities, and industry. Only by sharing our collective resources, ideas, and efforts can we solve these challenges and unlock tomorrow's greatest nanotechnology innovations.

Dr. Robert R. Doering is a Senior Fellow in Silicon Technology Development at Texas Instruments and is a member of the SIA's Technology Strategy Committee. Dr. Doering is one of the two U.S. representatives to the International Roadmap Committee, which governs the International Technology Roadmap for Semiconductors. In addition, he is a Fellow of the IEEE, has authored/presented more than 150 published/conference papers, and has 19 U.S. patents.